In The Claims:

1. (Currently Amended) A control chip for accelerating memory access, wherein said control chip is coupled to a system bus at least having a clocking line, said control chip comprising:

a memory write command queue for holding a plurality of memory write commands, wherein each said memory write command has a write address;

a bus interface unit coupled to the system bus, wherein said bus interface unit receives the first section read address and the second section read address of a memory read command sequentially from said system bus according to a clock signal and concurrently outputs said first section read address and said second section read address; and

a memory request organizer coupled to the bus interface unit and said memory write command queue for comparing said first section read address with an identical bit portion of **each** said write address of said memory-write commands inside said memory-write command queue;

wherein if the comparison indicates a difference, execution of said memory read command would be permitted; if the comparison indicates the presence of identical bits, said second section read address would be compared with an identical bit portion of **each** said write address of said memory-write commands inside said memory-write command queue;

wherein if the comparison indicates a difference, execution of said memory read command would be permitted; if said comparison still indicating said presence of identical bits,

permission to execute said memory read command would be delayed until [~~said~~]**the** memory-write command **with identical address bits** inside said memory-write command queue **executes**.

A2

2. (Currently Amended) The control chip of claim 1, wherein said memory request organizer further includes:

a first section address read/compare unit coupled to the bus interface unit and said memory-write command queue for receiving said first section read address, comparing said first section read address with an identical bit portion of said write address of said memory-write commands inside said memory-write command queue and outputting a first comparison signal;

a second section address read/compare unit coupled to the bus interface unit and said memory-write command queue for receiving said second section read address, comparing said second section read address with an identical bit portion of said write address of said memory-write commands inside said memory-write command queue and outputting a second comparison signal; and

a grant decision unit coupled to the first address read/compare unit and said second address read/compare unit for receiving said first comparison signal and said second comparison signal, determining and setting up a grant execution signal, wherein when either said first comparison signal or said second comparison signal indicates a difference, said grant execution signal is set, otherwise, said grant execution is set only after [~~said~~]**the** memory-write command **with identical address bits** inside said memory-write command queue **executes**.

3. (Original) The control chip of claim 2, wherein said memory request organizer further includes:

A2

a memory command control unit coupled to the grant decision unit for receiving said grant execution signal and outputting said memory read command directly or transferring said memory read command to a memory read command queue for storage.

4. (Currently Amended) The control chip of claim 1, wherein the rising edge and the falling edge of said clock signal are respectively defined as a bit time period, and two bit time periods **are** required to transfer said first section read address.

5. (Currently Amended) The control chip of claim 1[~~6~~], wherein said comparison of said first section read address with an identical bit portion of said write command includes comparing with bits 12 to 31 of said write address.

6. (Currently Amended) The control chip of claim 1[~~6~~], wherein said comparison of said second section read address with an identical bit portion of said write command includes comparing with bits 6 to 11 of said write address.

7. (Deleted)

8. (Currently Amended) A method of operating a control chip for accelerating memory access wherein said control chip couples with a system bus and includes at least a memory-write command queue for holding a plurality of memory-write commands with each said memory write command further including a write address, [,] said method comprising the steps of:

receiving [~~said~~]a first section read address transmitted through said system bus;

comparing said first section read address with an identical bit portion of **each** said write address of said memory-write commands inside said memory-write command queue;

A2

if the comparison indicate**s**[~~ing~~] some difference, permitting [~~said~~]execution of [~~said~~]**a** memory read command **associated with the first section read address;**

[~~to~~]receiv**ing**[~~e~~] said second section read address transmitted through said system bus;

comparing said second section read address with an identical bit portion of **each** said write address of said memory-write commands inside said memory-write command queue, and

if the comparison indicate**s**[~~ing~~] some difference, permitting said execution of said memory read command; and

if the comparison indicates [~~said~~]**a** presence of identical bits, waiting until said memory-write command inside said memory-write command queue, having an identical write address is executed before permitting said execution of said memory read command.

9. (Currently Amended) The method of claim **8**[~~10~~], wherein the rising edge and the falling edge of [~~said~~]**a** clock signal are respectively defined as a bit time period, and two bit time periods **are required** to transmit said first section read address.

AD
end

10. (Currently Amended) The method of claim **8**[~~10~~], wherein said memory read command is directly output or transferred to [~~the~~]**a** memory read command queue inside said control chip when execution of said memory read command is permitted.

11. (Currently Amended) The method of claim 10, wherein when a comparison between said first section read address and an identical bit portion of **each** said write address of said memory-write command**s** inside said memory-write command queue indicates some difference, a flag for permitting said execution of said memory read command is raised **immediately after totally receiving said memory read command**[~~during the first bit time period of said next read command~~].